5726

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format – Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 12/28/01 Serial # 09/863,927 Priority Application Date _____

Your Name M. Lewis Examiner # 7312

AU 2899 Phone 305-3543 Room _____

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: (USPT) DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

12-28-01 A11:12

BEST AVAILABLE COPY

Staff Use Only	Type of Search:	Vendors
Searcher: Derrick Blalock	Structure (#)_____	STN_____
Searcher Phone: 305-6933	Bibliographic_____	Dialog_____
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation_____	Questel/Orbit_____
Date Searcher Picked Up: 1/2/02	Fulltext_____	Lexis-Nexis_____
Date Completed: 1/22/02	Patent Family_____	WWW/Internet_____
Searcher Prep/Rev Time: 4hrs	Other_____	Other_____
Online Time: 210		

FIRST PASS WPIX, HCAPLUS

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FILE 'HCAPLUS, WPIX' ENTERED AT 09:34:04 ON 22 JAN 2002
L16           4 S (US6265765 OR US5688716 OR US5801441 OR US5518964)/PN
              SET SMARTSELECT ON
L17       SEL L16 1- IC MC :       33 TERMS
L18      217427 S L17
L19        4272 S L18 AND DIELECTRIC/TI,IT,ST
L20          75 S L19 AND (CURE######## OR CURAB? OR CURING)/TI,IT,ST
L21           2 S L20 AND COMPLIANT
L22           3 S (US 1997-62471P OR US1997-0062471 OR US 1998-166812 OR US 200
L23           3 S L20 AND ENCAPSULA?/TI,ST,IT
L24           2 S L23 NOT L21-22
L25        5594 S COMPLIANT
L26          25 S L19 AND L25
L27           5 S L26 AND (CURE######## OR CURAB? OR CURING)
L28           3 S L27 NOT L21-24
L29       92850 S RESILIENT
L30          14 S L29 AND L19
L31           2 S L30 AND (CURE######## OR CURAB? OR CURING)
L32           1 S L31 NOT (L21-24 OR L27-28)
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L22 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:434228 HCAPLUS
DN 133:36743
TI Methods of encapsulating a semiconductor chip for electronic packaging using a settable encapsulant
IN Distefano, Thomas H.; Mitchell, Craig S.
PA Tessera, Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-44
ICS H01L021-48; H01L021-50
NCL 438126000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 38
FAN.CNT 1

	PATENT NO.	KIND	DATE		APPLICATION NO.	DATE
PI	US 6080605	A	20000627		US 1998-166812	19981006 <--
	US 6218215	B1	20010417		US 2000-520357	20000307 <--
PRAI	US 1997-62471	P	19971015	<--		
	US 1998-166812	A3	19981006	<--		

AB A method of making a semiconductor chip package by attaching a chip to a dielec. layer; placing the dielec. layer and chip into a mold; disposing a thixotropic compn. that has been sheared to reduced its viscosity into the mold and curing the thixotropic compn. after the chip and dielec. layer were removed from the mold. A method of making a semiconductor chip package without using a mold by disposing a sheared thixotropic compn. between a semiconductor chip and a dielec. layer and then curing the thixotropic compn. to form a cured encapsulant. A method of making a semiconductor chip package without using a mold during the curing step and without the need to use a thixotropic compn. by placing a semiconductor chip attached to a dielec. layer into a mold and disposing a liq. compn. between the chip and the dielec. layer, forming a cured skin on the liq. compn., removing the workpiece from the mold and then completing the cure of the liq. compn.

ST encapsulating electronic package thixotropic encapsulant

IT Polyimides, uses
RL: NUU (Other use, unclassified); USES (Uses)
(dielec. film; methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant using)

IT Crosslinking
Molds (forms)
(in methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant)

IT Electronic packaging materials
Electronic packaging process
Potting
(methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant)

IT Dielectric films
(methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant and)

IT Thixotropic materials
(methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant as)

IT Epoxy resins, processes
Silicone rubber, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(methods of encapsulating semiconductor chip for electronic packaging

using settable encapsulant from)

IT Shear

(methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant using)

IT Gels

(silicone; methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant from)

IT Encapsulants

(thixotropic; methods of encapsulating semiconductor chip for electronic packaging using settable encapsulant)

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD

RE

(1) Baird; US 4996170 1991
(2) Distefano; US 5455390 1995
(3) Distefano; US 5518964 1996 HCAPLUS
(4) Distefano; US 5688716 1997 HCAPLUS
(5) Distefano; US 5776796 1998
(6) D'Entremont; US 5659652 1997
(7) Khandros; US 5148265 1992
(8) Kovac; US 5659952 1997
(9) Mitchell; US 5766987 1998
(10) Weld; US 5773322 1998 HCAPLUS

L16 ANSWER 2 OF 4 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-624248 [72] WPIX
CR 1996-097761 [10]; 1996-188719 [19]; 1998-007997 [01]; 1998-086369 [08]; 1998-378040 [32]; 1998-609264 [51]; 1999-370609 [31]; 1999-384095 [30]; 1999-561109 [47]; 2000-222146 [10]; 2000-464036 [38]; 2001-168218 [17]
DNN N2001-465068
TI Semiconductor chip assembly for complex microprocessor, has compliant layer with flexible leads electrically connected to terminals, extending up from chip contact to dielectric center region.
DC U11
IN DISTEFANO, T H; FARACI, T; SMITH, J W
PA (TESS-N) TESSERA INC
CYC 1
PI US 6265765 B1 20010724 (200172)* 16p H01L023-02 <--
ADT US 6265765 B1 Div ex US 1994-271768 19940707, CIP of US 1995-440665 19950515, Div ex US 1996-653016 19960524, US 1997-935962 19970923
FDT US 6265765 B1 Div ex US 5518964, Div ex US 5688716, CIP of US 5801441
PRAI US 1996-653016 19960524; US 1994-271768 19940707; US 1995-440665 19950515; US 1997-935962 19970923
IC ICM H01L023-02
AB US 6265765 B UPAB: 20011206
NOVELTY - A compliant layer supporting a dielectric sheet (52) above a sub-assembly (50), has flexible leads (62,64) which extend up from chip contact to dielectric center region and electrically connects the conductive terminals. The subassembly has a package such as heat sink, having a center region attached to chip and peripheral region extending out from chip.

USE - For complex microelectronic device such as complex microprocessor.

ADVANTAGE - The package provides good resistance to thermal stress, expansion and contraction of the substrate and chip. The assembly is readily tested and mounted to a substrate having different coefficient of thermal expansion.

DESCRIPTION OF DRAWING(S) - The figure shows the view depicting the elements of chip assembly at a later stage during the process.

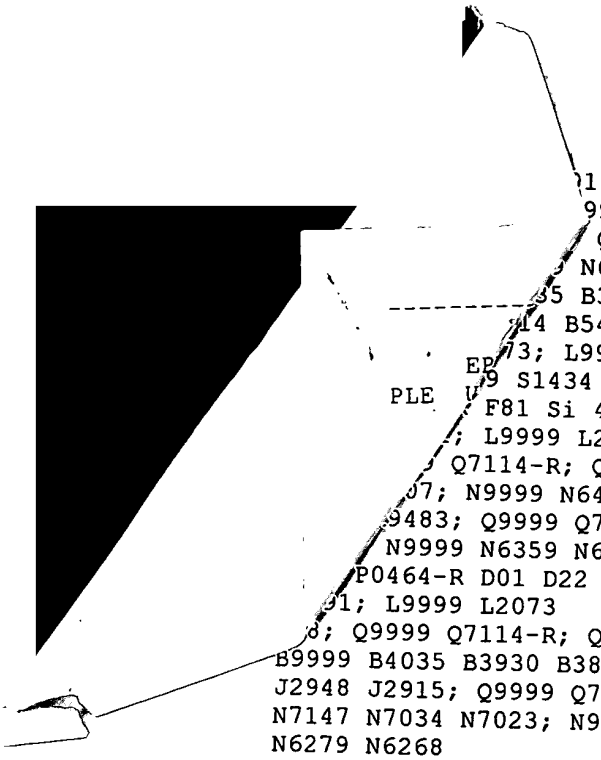
Sub-assembly 50

Dielectric sheet 52

Leads 62,64

Dwg.4/15
FS EPI
FA AB; GI
MC EPI: U11-D01A1

L22 ANSWER 3 OF 3 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-504959 [45] WPIX
CR 2001-281056 [29]
DNN N2000-373338 DNC C2000-151520
TI Encapsulation of semiconductor package, involves placing dielectric layer having microelectronic element in mold, sealing and filling sheared thixotropic component in mold, removing the layer and curing the component.
DC A26 A85 L03 U11
IN DISTEFANO, T H; MITCHELL, C S
PA (TESS-N) TESSERA INC
CYC 1
PI US 6080605 A 20000627 (200045)* 13p H01L021-44
ADT US 6080605 A **Provisional US 1997-62471P 19971015, US 1998-166812 19981006**
PRAI **US 1997-62471P 19971015; US 1998-166812 19981006**
IC ICM H01L021-44
ICS H01L021-48; H01L021-50
AB US 6080605 A UPAB: 20010528
NOVELTY - Microelectronic element(s) (20) disposed in dielectric layer (21), is placed in mold (23) and sealed. Thixotropic composition (28) is sheared to reduce its viscosity from initial viscosity. Sheared composition filled in between element(s) (20) and layer (21), is allowed for sufficient period of time to regain its initial viscosity. Layer (21) is removed, composition (28) is cured to form cured encapsulant.
USE - For encapsulating semiconductor chip package (claimed).
ADVANTAGE - The method without using mold during curing step and without the need to use thixotropic composition is provided. The method is provided for making plurality of semiconductor chip packages by dicing the package after curing of the package. The thixotropic composition prevents leaking or back flowing of the composition from the assembly when the mold is removed. The time and/or the energy required for making semiconductor chip package is reduced because the time needed for curing the encapsulant composition is reduced. Production of the package is raised by curing the encapsulant out of the mold, thereby production of packages is raised. The planarity of the package is maintained using a rigid platen which is fixed on the top surface of the frame during encapsulation and the adherence of cured encapsulant to platen is prevented. Encapsulant reduces and/or redistributes the strain and stress on the connections between semiconductor chip and the supporting substrate during operation of chip. The encapsulant seals the element against corrosion and insures intimate contact between the encapsulant, semiconductor chip and other element of the chip package. A void-free complaint layer in the final assembly is provided by filling the porous layer completely in the encapsulant.
DESCRIPTION OF DRAWING(S) - The figure depicts the side view of various steps of encapsulation of semiconductor chip package.
Microelectronic element 20
Mold 23
Thixotropic composition 28
Dwg.1-4/17
TECH US 6080605 A UPTX: 20000918
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Dielectric Layer: The dielectric layer comprising polyimide is flexible.
Preferred Thixotropic Composition: The thixotropic composition comprising silicone elastomers, silicon gels and flexible epoxy component is curable to form a encapsulant. The thixotropic composition has initial viscosity of above 150,000 centipoise at 25degreesC and reduced viscosity of below 10,000 centipoise at 25degreesC and the time required for the composition to regain at least 65% of its initial viscosity is less than 1 minute.
FS CPI EPI
FA AB; GI
MC CPI: A05-A01E2; A05-J01B; A06-A00E2; A11-B01; A12-E04; A12-E07C; L04-C20A



1; S9999 S1434
999 N6440-R; J9999 J2948 J2915; Q9999 Q7476
Q9999 Q7523; N9999 N7147 N7034 N7023; N9999
N6359 N6337; N9999 N6279 N6268; B9999 B3203-R
5 B3930 B3838 B3747; N9999 N7090 N7034 N7023;
4 B5403 B5276
3; L9999 L2391; L9999 L2073; P1445-R F81 Si 4A;
9 S1434
F81 Si 4A; S9999 S1365; S9999 S1434; M9999 M2073;
; L9999 L2073
Q7114-R; Q9999 Q9007; K9712 K9676; B9999 B3554-R;
7; N9999 N6440-R; J9999 J2948 J2915; Q9999 Q7476 Q7330;
9483; Q9999 Q7523; N9999 N7147 N7034 N7023; N9999 N7170
N9999 N6359 N6337; N9999 N6279 N6268
P0464-R D01 D22 D42 F47; S9999 S1434; M9999 M2073; L9999
1; L9999 L2073
; Q9999 Q7114-R; Q9999 Q9007; K9712 K9676; B9999 B3554-R;
B9999 B4035 B3930 B3838 B3747; ND01; ND07; N9999 N6440-R; J9999
J2948 J2915; Q9999 Q7476 Q7330; K9574 K9483; Q9999 Q7523; N9999
N7147 N7034 N7023; N9999 N7170 N7023; N9999 N6359 N6337; N9999
N6279 N6268

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L21 ANSWER 1 OF 2 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-281056 [29] WPIX
CR 2000-504959 [38]
DNN N2001-200387 DNC C2001-085362
TI Method of making a semiconductor chip package involves attaching a microelectronic element to a **dielectric** layer, placing a sheared thixotropic composition between the element and the **dielectric** layer and **curing** the thixotropic composition.
DC A85 L03 U11
IN DISTEFANO, T H; MITCHELL, C S
PA (TESS-N) TESSERA INC
CYC 1
PI US 6218215 B1 20010417 (200129)* 13p H01L021-44 <--
ADT US 6218215 B1 Provisional US 1997-62471P 19971015, Div ex US 1998-166812 19981006, US 2000-520357 20000307
FDT US 6218215 B1 Div ex US 6080605
PRAI US 1997-62471P 19971015; US 1998-166812 19981006; US 2000-520357 20000307
IC ICM **H01L021-44**
ICS H01L021-48; H01L021-50
AB US 6218215 B UPAB: 20010528
NOVELTY - Method of making a semiconductor chip package comprises: (a) attaching at least one microelectronic element to a dielectric layer; (b) shearing a thixotropic composition to reduce its viscosity; (c) placing the thixotropic composition (28) between the microelectronic element(s) and the dielectric layer; and (d) curing the thixotropic composition to form a cured encapsulant.
USE - The method can be used for packaging a semiconductor chip or an entire wafer with an encapsulant.
DESCRIPTION OF DRAWING(S) - The diagram shows a side view of the workpiece and mold after the workpiece has been removed from the mold and the thixotropic encapsulant composition has subsequently been cured to form a cured encapsulant.
Thixotropic composition 28
Dwg.4/17
TECH US 6218215 B1 UPTX: 20010528
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method further comprises: (e) attaching the dielectric layer to a frame before step (c). Step (e) is performed before step (a).
The dielectric sheet is placed on the bottom surface of the frame, the front surface of the microelectronic element(s) faces the dielectric sheet and the method further comprises: (f) attaching a coverlay to the bottom surface of the frame so that the coverlay is disposed over the back surface of the microelectronic element.
Steps (b) and (c) are partially carried out simultaneously or are completed at the same time. Step (b) is completed before step (c) or vice versa.
At least one microelectronic element is a semiconductor chip. At least one microelectronic element is a wafer.

TECHNOLOGY FOCUS - POLYMERS - Preferred Materials: The dielectric sheet is flexible. The dielectric sheet comprises polyimide. The thixotropic composition is curable to form a **compliant** encapsulant selected from silicone elastomers, silicone gels and flexibilized epoxies.
Preferred Properties: The initial viscosity of the thixotropic composition more than 150,000 centipoise at 25 degreesC, the reduced viscosity less than 10,000 centipoise at 25 degreesC and the time required for the thixotropic composition to regain at least 65% of its initial viscosity is less than 1 minute.
FS CPI EPI
FA AB; GI
MC CPI: A99-A; L04-C20A

L32 ANSWER 1 OF 1 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1989-229419 [32] WPIX
DNN N1989-175001
TI Passivation for conventional integrated circuits - forming hard **dielectric** layer over conductor elements followed by viscous layer which, when **cured**, receives further hard layer.
DC U11
IN GENOT, B; MERENDA, P
PA (SGSA) SGS-THOMSON MICROEL; (SGSA) SGS THOMSON MICROELTRN SA
CYC 5
PI EP 327412 A 19890809 (198932)* EN 8p
R: DE GB IT
FR 2625839 A 19890713 (198935)
JP 01225326 A 19890908 (198942)
EP 327412 B1 19940921 (199436) FR 7p H01L023-28
R: DE GB IT
DE 68918301 E 19941027 (199442) H01L023-28
ADT EP 327412 A EP 1989-400042 19890106; JP 01225326 A JP 1989-7537 19890113; EP 327412 B1 EP 1989-400042 19890106; DE 68918301 E DE 1989-618301 19890106, EP 1989-400042 19890106
FDT DE 68918301 E Based on EP 327412
PRAI FR 1988-294 19880113
REP DE 3030862; EP 34455; FR 2382095; GB 1566072; JP 57031145; JP 57088734; JP 57199224; JP 58974043; JP 61079233; JP 61154131; JP 61232646; US 4198444; 9.Jnl.Ref; JP 58074043
IC H01L021-31; H01L023-28
ICM H01L023-28
ICS H01L021-31; H01L021-314; **H01L021-56**
AB EP 327412 A UPAB: 19930923
An integrated circuit is coated in the usual way with a hard dielectric layer (9) to provide protection. This tends to follow the contours of the circuit's conductor elements (8) which stand proud of its surface, an undulating upper face thus developing. This face is covered with a silica-based gel known as "Spin-on Glass" which is subsequently **cured** at an appropriate temperature to extract its suspension solvent. A less undulating **resilient** surface results, and may be lightly plasma-treated to improve its profile.

The process is normally completed by depositing a further hard dielectric layer on top, a substantially level surface being achieved. Further depositions of gel and hard dielectric may follow, the **cured** gel layers enhancing resistance of the circuit beneath to externally-imposed stresses.

ADVANTAGE - Use of alternating hard and **cured** viscous layers introduces resilience into structure which protects circuit beneath from fractures due to external stresses.

1/4
FS EPI
FA AB; GI

L24 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:488823 HCAPLUS
DN 103:88823
TI **Encapsulation** of semiconductor devices
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM **H01L021-56**
ICS C08G059-68; H01L023-30
CC 38-3 (Plastics Fabrication and Uses)
Section cross-reference(s): 76
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 60072235	A2	19850424	JP 1983-179122	19830929

AB A semiconductor device is passivation-coated with a photocurable epoxy resin compn. contg. an Al compd. and a silicon compd. which gives a silanol upon irradn. before encapsulation with an epoxy resin to give a moisture-resistant product at high prodn. rate. Thus, a semiconductor device was coated with a compn. comprising Epikote 828 [25068-38-6] 20, ERL 4221 [25085-98-7] (alicyclic epoxy resin) 80, tris(acetylacetonato)aluminum [13963-57-0] 0.5, and tert-butylperoxytriphenylsilane [18751-58-1] 2 parts, UV-cured, and encapsulated with MP 3000 (epoxy resin) to give a product having no defective samples after 150 h in a pressure cooker with 120.degree.-steam at 2 atm., compared with 100% failure for samples precoated with a siloxane.

ST photocurable epoxy resin passivation coating; potting semiconductor device passivation coating; acetylactonatoaluminum photocurable epoxy resin; butylperoxytriphenylsilane photocurable epoxy resin; aluminum acetylacetonate photocurable epoxy resin

IT Potting
(compns., epoxy resins, for semiconductor devices, passivation coatings for, photocurable epoxy resins as, with high moisture resistance)

IT Semiconductor devices
(passivation of, with photocurable epoxy resins, in manuf. of **encapsulated** products with high moisture resistance)

IT Electric insulators and **Dielectrics**
(photocurable epoxy resins, in passivation of semiconductor devices, for **encapsulated** products with high moisture resistance)

IT Epoxy resins, uses and miscellaneous
RL: USES (Uses)
(photocurable, semiconductor devices passivation-coated with, for **encapsulated** products with high moisture resistance)

IT Crosslinking catalysts
(photosensitive silanes, for epoxy resins, in passivation coating of semiconductor devices)

IT 18751-58-1 88216-14-2 88216-15-3
RL: CAT (Catalyst use); USES (Uses)
(**curing** catalysts, photosensitive, epoxy resins contg., semiconductor devices passivation-coated with, for **encapsulated** products with high moisture resistance)

IT 13963-57-0 14325-56-5 15306-17-9
RL: USES (Uses)
(photocurable epoxy resins contg., semiconductor devices passivation-coated with, for **encapsulated** products with high moisture resistance)

IT 25068-38-6 25085-98-7 91372-01-9
RL: USES (Uses)
(photocurable, semiconductor devices passivation-coated with, for

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L16 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:279602 HCAPLUS
TI Enhancements in framed sheet processing
IN Beroz, Masud; Distefano, Thomas H.; Hendrickson, Matthew T.; Light, David; Smith, John W.
PA Tessera, Inc., USA
SO U.S., 27 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM B32B001-04
ICS H01L021-02
NCL 428068000
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6217972	B1	20010417	US 1998-173797	19981016
	US 5518964	A	19960521	US 1994-271768	19940707 <--
	US 5798286	A	19980825	US 1995-532528	19950922
	US 5688716	A	19971118	US 1996-653016	19960524 <--
	US 5913109	A	19990615	US 1996-690532	19960731
	WO 9711486	A1	19970327	WO 1996-US15170	19960923
	AU 9672425	A1	19970409	AU 1996-72425	19960923
	EP 853816	A1	19980722	EP 1996-933850	19960923
	CN 1197544	A	19981028	CN 1996-197128	19960923
	WO 9828955	A2	19980702	WO 1997-US23949	19971212
	WO 9828955	A3	19980903		
	AU 9862374	A1	19980717	AU 1998-62374	19971212
	US 5989936	A	19991123	US 1997-989312	19971212
	US 6104087	A	20000815	US 1998-138858	19980824
	US 6117694	A	20000912	US 1999-267058	19990312
	US 6080603	A	20000627	US 1999-268286	19990315
	US 6194291	B1	20010227	US 1999-372021	19990809
	US 6307260	B1	20011023	US 1999-395105	19990914
	US 6338982	B1	20020115	US 2000-688397	20001016
	US 2001000032	A1	20010315	US 2000-727161	20001130
	US 2001050425	A1	20011213	US 2001-781374	20010212
PRAI	US 1997-61932	P	19971017		
	US 1994-271768	A3	19940707		
	US 1994-366236	B2	19941229		
	US 1995-440665	A2	19950515		
	US 1995-1782	P	19950802		
	US 1995-532528	A	19950922		
	US 1996-1718	P	19960731		
	US 1996-690532	A1	19960731		
	WO 1996-US15170	W	19960923		
	US 1996-32828	P	19961213		
	US 1997-885238	A2	19970630		
	US 1997-989312	A2	19971212		
	WO 1997-US23949	W	19971212		
	US 1998-77928	P	19980313		
	US 1998-57125	A1	19980408		
	US 1998-138858	A2	19980824		
	US 1998-173797	A3	19981016		
	US 1998-174074	A3	19981016		
	US 1999-330859	A1	19990611		

AB A flexible sheet used in manufacture of microelectronic components is held on a frame formed from a rigid material so that the frame maintains the sheet under tension during processing and thereby stabilizes the dimensions of the sheet. The frame may be formed from a rigid, light-transmissive material such as a glass, and the bond between the frame and sheet may be made or released by light transmitted through the

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     FILE 'HCAPLUS, JAPIO, WPIX' ENTERED AT 10:31:20 ON 22 JAN 2002
L1      1026422 S IC OR ICS OR INTEGRATED(W)CIRCUIT# OR (MICRO)(W)(CIRCUIT# OR
L3      1289155 S H01L?/IC
L4      3068869 S DIELECTRIC? OR OXIDE OR INSULAT?
L5       412471 S CURING OR CURABLE OR CURE OR CURED
L6      7086876 S LIQUID# OR FLUID# OR SOL# OR SOLUTION# OR SOLN
L7        18653 S H01L-021/56/IC
L8      2077873 S L1 OR L3
                SET SMARTSELECT ON
L9       268453 S L8 AND (PACKAGE? OR ENCAS##### OR PROTECT? OR CASING OR CASE
L10       61267 S L9 AND L4
L11          44 S L10 AND (L5(3N)L6)
L12          44 DUP REMOVE L11 (0 DUPLICATES REMOVED)
```

frame. Preferred features of the framed sheet minimize entrapment of processing liquids such as etch solutions, thereby minimizing carryover of processing solutions between steps. The frame may have contact openings which permit engagement of a metallic layer on the sheet by an electrode carrying electroplating or etching current without disturbing the main portion of the sheet where features are to be formed or treated.

D L12 BIB AB 1-3

L12 ANSWER 1 OF 44 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:380971 HCAPLUS
DN 134:374826
TI Method for producing a support element for an **integrated circuit** (**IC**) component
IN Senge, Carsten; Staudt, Mathias; Mentzer, Ruediger
PA Orga Kartensysteme G.m.b.H., Germany
SO PCT Int. Appl., 14 pp.
CODEN: PIXXD2
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2001037621	A2	20010525	WO 2000-DE3930	20001110

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD,

PRAI DE 1999-19955537 A 19991118
AB The invention relates to a method for producing a support element for an **integrated circuit** component which is to be included in a data carrier card. Conductor strips which have contact surfaces on both resp. flat sides of the support element are etched out of a conductive layer. One side of the contact surface is connected to a resp. connecting contact of the **IC** component and the other side serves as an external contact. The external contact surfaces and their corresponding conductor strips are coated with an addnl. elec. conductive **protective** layer. During a 1st step of the method, the elec. conductive layer is coated with a **liq**. or pasty **curable** coating material on one flat side on the contact surface points which have been provided to make the connecting contact. The remaining uncoated surface regions of the flat side are then coated with a **liq**. or pasty **curable** nonconductive material. In subsequent steps of the method, the conductor strips and contact surfaces are etched out of elec. conductive layer and are coated with the addnl. elec. conductive **protective** layer. In the final step of the method, the coating material which has been applied only to one side is removed. The inventive method produces a support element which lacks the conventional support film usually used for the elec. conductive layer. This leads to a redn. in the height of the unit formed by the **IC** component and support element, despite a slightly thicker elec. conductive layer achieved by a corresponding material compn. of the Cu foil which is preferably used.

L12 ANSWER 2 OF 44 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:582295 HCAPLUS
DN 135:145737
TI Semiconductor processing methods of forming encapsulant over semiconductive **dies**, and methods of forming **die packages**
IN Grigg, Ford B.; Brand, Joseph M.
PA USA
SO U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

01/22/2002

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001012641	A1	20010809	US 1999-360785	19990726

AB The invention pertains to methods of forming encapsulant over semiconductor **dies**, such as, for example, methods of forming **die packages**. In one aspect, the invention encompasses a semiconductor processing method. An **insulative** substrate is provided. Such substrate has an opening extending through it. A semiconductor-material-comprising **die** is provided adjacent to the substrate, and the **die** has an edge. A gap is between the **die** and substrate, and exposed through the opening. A **liq** . radiation-**curable** material is flowed through the opening and into the gap. Radiation is directed from beside the **die** to cure at least a portion of the radiation-curable material within the gap and thus form a dam which impedes non-cured radiation-curable material from flowing beyond the edge. In another aspect, the invention encompasses a method of forming a **die package**. An **insulative** substrate is provided. Circuitry is over a topside of the substrate, and a slit extends through the substrate. A semiconductive-material-comprising **die** is provided beneath the substrate, and has a surface exposed through the slit in the substrate. The **die** has an edge. There is a gap between the **die** and an underside of the substrate. A radiation-curable material is injected through this slit and into the gap. Radiation is directed from over the edge to the gap to cure at least a portion of the radiation-curable material within the gap and thus form a dam which impedes non-cured radiation-curable material from flowing beyond the edge.

L12 ANSWER 6 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-256195 [26] WPIX
DNN N2001-182597 DNC C2001-077060
TI Manufacture of anisotropic conductive element for microelectronic packaging by providing conductive material layer containing **dielectric** material and conductive particles, and applying electromagnetic field.
DC A32 A85 L03 P81 U11 U14
IN HABA, B
PA (TESS-N) TESSERA INC
CYC 1
PI US 6190509 B1 20010220 (200126)* 20p
ADT US 6190509 B1 Provisional US 1997-40021P 19970304, US 1998-34515 19980304
PRAI US 1997-40021P 19970304; US 1998-34515 19980304
AB US 6190509 B UPAB: 20010515
NOVELTY - An anisotropic conductive element is manufactured by providing a conductive material layer (28) incorporating curable **dielectric** material (30) in fluid condition and electrically conductive particles (32) in the **dielectric** material; applying an electromagnetic field to the layer; and curing the **dielectric** material.
DETAILED DESCRIPTION - Manufacture of an anisotropic conductive element comprises:
(a) providing a layer of material having opposed faces;
(b) applying an electromagnetic field to the layer; and (c) curing the **dielectric** material. The layer of material incorporates a **curable dielectric** material in **fluid** condition and an electrically conductive particles in the **dielectric** material. The electromagnetic field alters the configuration of the particles and forms areas of high-particle concentration defining conductive paths extending between the major faces.

L12 ANSWER 7 OF 44 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:434228 HCAPLUS
DN 133:36743
TI Methods of **encapsulating** a semiconductor **chip** for electronic packaging using a settable encapsulant
IN Distefano, Thomas H.; Mitchell, Craig S.
PA Tessera, Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6080605	A	20000627	US 1998-166812	19981006
	US 6218215	B1	20010417	US 2000-520357	20000307
PRAI	US 1997-62471	P	19971015		
	US 1998-166812	A3	19981006		

AB A method of making a semiconductor **chip package** by attaching a **chip** to a **dielec**. layer; placing the **dielec**. layer and **chip** into a mold; disposing a thixotropic compn. that has been sheared to reduced its viscosity into the mold and curing the thixotropic compn. after the **chip** and **dielec**. layer were removed from the mold. A method of making a semiconductor **chip package** without using a mold by disposing a sheared thixotropic compn. between a semiconductor **chip** and a **dielec**. layer and then curing the thixotropic

compn. to form a cured encapsulant. A method of making a semiconductor **chip package** without using a mold during the curing step and without the need to use a thixotropic compn. by placing a semiconductor **chip** attached to a **dielec.** layer into a mold and disposing a liq. compn. between the **chip** and the **dielec.** layer, forming a **cured** skin on the **liq** . compn., removing the workpiece from the mold and then completing the **cure** of the **liq.** compn.

L12 ANSWER 8 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-685985 [67] WPIX
DNN N2000-507093 DNC C2000-208615
TI **Encapsulation** of microelectronic assembly involves curing a barrier layer while in contact with exterior surfaces to form a layer that will cover apertures.
DC A32 A85 L03 U11 U14
IN FJELSTAD, J; SMITH, J W
PA (TESS-N) TESSERA INC
CYC 1
PI US 6130116 A 20001010 (200067)* 13p <--
ADT US 6130116 A Provisional US 1996-32871P 19961213, US 1997-984933 19971204
PRAI US 1996-32871P 19961213; US 1997-984933 19971204
AB US 6130116 A UPAB: 20010502
NOVELTY - A microelectronic assembly (30) is **encapsulated** by curing a barrier layer (32) on a supporting element (36) to form a layer that will cover the apertures, applying a **curable liquid** encapsulant (40) to the microelectronic assemblies, and curing the encapsulant. The barrier layer maintains in contact with the exterior surface (22) as curing process occurs.

DETAILED DESCRIPTION - **Encapsulating** a microelectronic assembly comprises:

(a) providing microelectronic assemblies having elements (12, 14) e.g. semiconductor **chip** and flexible **dielectric** sheet which defines exterior surfaces and an array of terminals (24) exposed at the exterior surfaces;

(b) providing a barrier layer on a supporting element;

(c) assembling the supporting element and the microelectronic elements for the layer to contact to the exterior surfaces and to cover apertures;

(d) curing the barrier layer while maintaining the barrier layer in contact with the exterior surfaces to form a layer which covers the apertures;

(e) applying a **curable liquid** encapsulant to the microelectronic assemblies; and

(f) curing the encapsulant.

The microelectronic elements define apertures through the exterior surfaces. The barrier layer has openings (38) aligned to the terminals. The layer on a surface of the supporting element is provided by screen-printing.

USE - The method is used for **encapsulating** a microelectronic assembly.

=> D L12 BIB AB 9-44

L12 ANSWER 9 OF 44 JAPIO COPYRIGHT 2002 JPO
AN 1999-297827 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN YOSHIMORI MASANORI
PA NEC KYUSHU LTD
PI JP 11297827 A 19991029 Heisei
AI JP1998-101507 (JP10101507 Heisei) 19980413
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
AB PROBLEM TO BE SOLVED: To considerably reduce parasitic capacity generated between wirings, by forming the silica layer of silicon **oxide** hydroxide whose relative **dielectric** constant is smaller than that of a silicon **oxide** film on the upper part of a **cavity** having upper/lower ends corresponding to the thickness of the metal wiring.
SOLUTION: A prescribed quantity of silica solution (silicon **oxide** hydroxide whose relative **dielectric** constant is smaller than a silicon **oxide** film) is previously stored in a storage liquid plate. A semiconductor substrate 101 is upset and it is supported by the base member and is lowered. Movement is stopped in a position where a part from a silicon **oxide** film 108 to the silicon **oxide** films 107 is immersed into silica solution. It is immersed into silica solution for prescribed time and the base member is pulled upward. Silica solution is held between the metal wirings by surface tension, and the upper opening part of a groove is covered by silica solution. When the semiconductor substrate 101 is baked in a state where it is vertically raised from silica solution, held silica **solution** is **cured** and a silica layer 109 is formed at the upper part of the groove between the silicon **oxide** films 107, and **cavities** 110 are formed by them.

L12 ANSWER 12 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-579451 [49] WPIX
DNC C1999-168501
TI Producing elongated foam-containing structure having **insulating** properties by pulling hollow, impermeable carrier through pultrusion **die**.
DC A32 A35 A94
IN GRINSHPUN, V S; HULLS, B; SPOO, K J; GRINSHPUN, V; SPOO, K
PA (OWEN) OWENS-CORNING FIBERGLAS TECHNOLOGY INC; (OWEN) OWENS CORNING
CYC 87
PI US 5955013 A 19990921 (199949)* 15p
WO 2000003858 A1 20000127 (200013) EN
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB
AB US 5955013 A UPAB: 19991124
NOVELTY - Foam-containing structure is produced by applying a defoamer (38) to the surface of a **cavity** in an elongated, hollow, impermeable carrier (12) before introducing foamed resin (46) and curing it. The defoamer causes foam contacting it to form a liquid layer so that the structure produced has a foamed resin inner core and a solid resin outer layer surrounding its sides.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for producing a foam-containing structure using a permeable carrier. In this **case**, a defoamer and a catalyst is applied to the **cavity** surface to produce a rapidly **curing liquid** resin layer

impregnating the carrier and preventing the foamed resin, subsequently curing, from flowing outwards.

USE - For producing a foam-containing structure having **insulating** properties. By implication and illustration, it may be used for producing a foam filled, solid skinned **insulation** strip.

L12 ANSWER 13 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-492848 [41] WPIX
DNN N1999-367025 DNC C1999-144324
TI Production of semiconductor **chip** assembly with enhanced **encapsulation** and reduced stress.
DC A35 A85 L03 U11
IN DISTEFANO, T H
PA (TESS-N) TESSERA INC
CYC 1
PI US 5937276 A 19990810 (199941)* 13p <--
ADT US 5937276 A Provisional US 1996-33075P 19961213, US 1997-947180 19971008
PRAI US 1996-33075P 19961213; US 1997-947180 19971008
AB US 5937276 A UPAB: 19991011
NOVELTY - A semiconductor **chip** assembly having enhanced **encapsulation** is formed by providing a support with a **dielectric** layer and an overlying bus (32) to which leads (44) are attached. A **chip** (50) is brought up, the leads detached from the bus and bonded to the contacts (54) and a liquid flowed between **chip** and support and cured.

DETAILED DESCRIPTION - Manufacture of a semiconductor **chip** assembly comprises providing a connection component including a support having a **dielectric** top surface and central (26) and peripheral (28) portions with a gap (20). A bus (32) overlies the periphery and gaps of the support and electrical leads (44) overlie the top surface having one end secured to the central portion and the other to the bus. A **chip** (50) is placed with its front, contact, face opposed to the bottom of the support, leads are detached and displaced from the bus and bonded to the contacts (54) and a **curable liquid** is flowed between the **chip** and support, wetting the inner edge of the bus and then cured.

L12 ANSWER 15 OF 44 JAPIO COPYRIGHT 2002 JPO
AN 1998-261741 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE OF SEMICONDUCTOR DEVICE
IN MORINAGA YUICHI
PA OKI ELECTRIC IND CO LTD, JP (CO 000029)
PI JP 10261741 A 19980929 Heisei
AI JP1997-66737 (JP09066737 Heisei) 19970319
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 9
AB PURPOSE: TO BE SOLVED:To enable a connecting metal fine wire to be prevented from being separated from an inner lead or to be **protected** against disconnection at molding with sealing resin by a method wherein the joint between a wire such as the metal fine wire and the inner lead is coated with **insulating** resin other sealing **insulating** resin.
CONSTITUTION: r leads 4 are formed adjacent to a semiconductor element 2, a metal fine wire 5 as a wire is provided and electrically connected between the connecting parts, for instance, the connecting pads of the inner lead 4 and the semiconductor element 2. After the metal fine wire 5 is connected, liquid **insulating** resin 7 different from sealing **insulating** resin is discharged out onto an **insulating** resin board through a nozzle 6 so as to coat, at least, a joint between

the metal fine wire 4 and the inner lead 4. That is, a joint between the metal fine wire 5 and the semiconductor element 2 and all the metal fine wire 5 besides the joint between the metal fine wire 4 and the inner lead 4 are coated with **cured liquid insulating** resin 7.

L12 ANSWER 16 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-130931 [12] WPIX
DNN N1998-103291 DNC C1998-043340
TI Securing lead frame to heat dissipating base in **integrated circuit** - by forming layer of thermoplastic adhesive on frame, contacting with non-conductive microspheres, pressing base against layer and curing.
DC A85 L03 U11
IN ALERING, T; ROSS, R J
PA (RJRP-N) RJR POLYMERS INC
CYC 78
PI WO 9805067 A1 19980205 (199812)* EN 16p <--
RW: AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
AU 9737420 A 19980220 (199828) <--
TW 376573 A 19991211 (200043) <--
ADT WO 9805067 A1 WO 1997-US13324 19970725; AU 9737420 A AU 1997-37420 19970725; TW 376573 A TW 1997-110774 19970729
FDT AU 9737420 A Based on WO 9805067
PRAI US 1997-896596 19970718; US 1996-22723P 19960729
AB WO 9805067 A UPAB: 19980323
A method of securing a lead frame to a heat dissipating base member in an **integrated circuit package** to give a **dielectric** bond comprises pressing a lead frame or a base member, on one of which is formed a layer of **curable liquid** adhesive with a tacky exposed surface contacted with electrically non-conductive microspheres to cause a layer of microspheres no more than microsphere thick to adhere to the tacky exposed surface, against the layer of microspheres to cause the microspheres to penetrate the adhesive and contact both the lead frame and the base member. The adhesive is then cured to join the lead frame to the base member while maintaining a separation between them whose thickness is equal to the diameter of one of the microspheres.

L12 ANSWER 17 OF 44 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:310095 HCAPLUS
DN 126:278693
TI **Dielectric** liquid epoxy resin compositions for injection moldings and their **packaged** electric devices
IN Fujiura, Hiroshi
PA Toshiba Chem Prod, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09059353	A2	19970304	JP 1995-237820	19950823

AB The elec. devices are **packaged** with **cured** products of **liq**. epoxy resin compns. contg. acid anhydrides, curing accelerators, and montanic acid or their ester derivs. as additive mold releasing agents. Thus, a liq. compn. comprising bisphenol A diglycidyl ether 100, SiO2 300, a silane coupling agent 0.5, methylhexahydrophthalic anhydride 90, 1,2-dimethylimidazole 2, and Hoechst Wax E 3 parts was injection-molded into a molding wherein a coil was set and cured to gived test pieces showing good mold releasability.

L12 ANSWER 18 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-007997 [01] WPIX
CR 1996-097761 [10]; 1996-188719 [19]; 1998-086369 [08]; 1998-378040 [32]; 1998-609264 [51]; 1999-370609 [31]; 1999-384095 [30]; 1999-561109 [47]; 2000-222146 [10]; 2000-464036 [38]; 2001-168218 [17]; 2001-624248 [49]
DNN N1998-006352 DNC C1998-002757
TI Manufacturing a fan-out semiconductor **chip** assembly - comprises mounting and handling **chip** using surface mounting techniques, connecting **chip** on **dielectric** element with flexible leads and injecting curable resin.
DC A85 L03 U11
IN DISTEFANO, T H; FARACI, T; SMITH, J W
PA (TESS-N) TESSERA INC
CYC 1
PI US 5688716 A 19971118 (199801)* 16p <--
ADT US 5688716 A Div ex US 1994-271768 19940707, CIP of US 1995-440665 19950515, US 1996-653016 19960524
FDT US 5688716 A Div ex US 5518964
PRAI US 1996-653016 19960524; US 1994-271768 19940707; US 1995-440665 19950515
AB US 5688716 A UPAB: 20011211
Making a semiconductor **chip** assembly comprises: (a) providing a sub-assembly including a semiconductor **chip** having a front surface and having contacts on the front surface, and a **package** element attached to the **chip** so that a peripheral region of the **package** element projects outwardly away from the **chip** in horizontal directions generally parallel to the front face of the **chip**; (b) providing a **dielectric** element having top and bottom surfaces and terminals on the top surface, and positioning the **dielectric** element to overlie the sub-assembly with the top surface and terminals facing away from the **chip** and **package** element, with a central region of the **dielectric** element disposed adjacent the **chip** and with a peripheral region of the **dielectric** element carrying at least some of the terminals overlying the peripheral region of the **package** element; (c) providing first leads attached to the **chip** at one end thereof and to the **dielectric** element at the other end thereof, the first leads being electrically connected between the contacts of the **chip** and the terminals on the **dielectric** element; (d) moving the **dielectric** element and **chip** relative to one another through a predetermined displacement so that the **dielectric** element moves with a vertical component of motion away from the **chip**, and so that the first leads are bent to a configuration in which each first lead is flexible; and (e) injecting a **curable liquid** beneath the **dielectric** element and **curing** the **liquid** to form a compliant layer supporting the **dielectric** element above the **chip** and **package** element

L12 ANSWER 20 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1997-086053 [08] WPIX
DNN N1997-070922 DNC C1997-027959
TI **Integrated circuit** passivation to prevent moisture and floating ion ingress - forming one passivation on **integrated circuit** containing non-planar structure and at least one conductive sheet.
DC L03 U11
IN HWANG, J; JAN, B; WANG, M; YAN, L
PA (MACR-N) MACRONIX INT CO LTD
CYC 1
PI TW 288195 A 19961011 (199708)* 28p <--
ADT TW 288195 A TW 1995-108731 19950821
PRAI TW 1995-108731 19950821
AB TW 288195 A UPAB: 19970220
A process of **integrated circuit** passivation, which forms one passivation on **integrated circuit** containing non-planar structure and at least one conductive sheet, comprises: (1) depositing first **dielectric** on **integrated circuit**; (2) coating one fluid **dielectric** on first **dielectric**, in which the fluid **dielectric** is formed by coating one fluid glass by spinning and curing on first **dielectric** and making the below structure represent planarised surface, and decreasing thickness of **cured fluid** glass without removing by eroding; (3) depositing third and fourth **dielectric** on fluid **dielectric**, in which the third and fourth **dielectric** contains one pair of isotropically wet etched PSG with higher eroding rate, time length of eroding process must control so as to avoid SiON being punched through to **protect** fluid **dielectric**, and PSG deposited by plasma chemical vapour on the fourth **dielectric** adopts plasma synthesis on depositing; (4) on the fourth **dielectric** overlaying on photoresist mask with opening of conductive sheet, on which the thickness of fluid glass is less than 0.05 mum; (5) removing the fourth and one portion of third **dielectric** in the above opening by isotropic wet etching process; (6) by anisotropic dry etching removing left **dielectric** in the above opening, which includes on portion of third **dielectric**, fluid **dielectric** and first **dielectric**, until

L12 ANSWER 22 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1995-390361 [50] WPIX
DNN N1995-285004 DNC C1995-167935
TI Semiconductor having good heat and solvent resistance - comprises semiconductor element opt. contg. **insulators** on surface contg. polyimide resin layers on its **insulators**.
DC A26 A85 L03 U11
PA (TOSM) TOSHIBA CHEM CORP
CYC 1
PI JP 07268099 A 19951017 (199550)* 5p
ADT JP 07268099 A JP 1994-89122 19940404
PRAI JP 1994-89122 19940404
AB JP 07268099 A UPAB: 19951215
Semiconductors comprises a semiconductive element, opt. contg. **insulators** on its surface, contg. polyimide resin layers on its **insulators**, obtd. by **curing** polyamic acid **soln**. composed of (A) and (B). 1-30 mol.% of diamine component composed of (A) and/or (B) is diaminosiloxane of formula (I), and (B) in the soln. is 20-50 wt.%. (A) = Polyamic acid soln. prepd. by reaction of

3,3',4,4'-biphenyl tetracarboxylic dianhydride, and paraphenylene diamine; and (B) = polyamic acid soln. prepd. in reaction of pyromellitic dianhydride and 4,4'-diamino diphenyl ether. R1,R2 = divalent organic base; R3-R6 = 1-6C hydrocarbon base and n = 0-12.

L12 ANSWER 24 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1995-007093 [01] WPIX
CR 1997-489910 [45]
DNN N1995-005734
TI Multi-**chip** module packaging and interconnection structure for **integrated circuit** - forms **cavities** to hold **die**, and bonds **die** pads to I-O pads using thermo-sonic bonding.
DC U11 U14 V04
IN GRISWOLD, B L; HO, C W; ROBINETTE, W C
PA (MICR-N) MICROMODULE SYSTEMS INC; (MICR-N) MICROMODULE SYSTEMS
CYC 18
PI WO 9427318 A1 19941124 (199501)* EN 34p <--
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: DE GB JP
US 5422514 A 19950606 (199528) 14p
US 5998859 A 19991207 (200004) <--
ADT WO 9427318 A1 WO 1994-US5172 19940510; US 5422514 A US 1993-60406 19930511; US 5998859 A Cont of US 1993-60406 19930511, US 1995-420844 19950410
FDT US 5998859 A Cont of US 5422514
PRAI US 1993-60406 19930511; US 1995-420844 19950410
AB WO 9427318 A UPAB: 20000124
The packaging structure includes a thin film multilayer interconnect circuit on a baseplate. The baseplate includes a **chip** mounting **cavity**. The circuit has one layer including several bonding pads on one surface, a second layer including several other bonding pads on a second surface, and a routing layer which includes several routing conductors. An **integrated circuit** dia. within the **cavity** has several input-output pads in contact with the first surface of the interconnect circuit.

The **die** is aligned so as to mate the input-output pads with the first set of bending pads. The pads are thermo-sonically bonded. A layer of encapsulant is placed over the **die**.

L12 ANSWER 25 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1994-176379 [21] WPIX
CR 1996-496450 [49]
DNN N1994-138900 DNC C1994-080753
TI Electronic devices **encapsulated** in vinyl/hydride terminated silicone resin - the vinyl/hydride ratio ensuring resin remains **liq** even after **cure**.
DC A85 L03 U11
IN WONG, C
PA (AMTT) AMERICAN TELEPHONE & TELEGRAPH CO; (AMTT) AT & T BELL LAB
CYC 2
PI US 5317196 A 19940531 (199421)* 5p <--
JP 06177279 A 19940624 (199430) 4p <--
ADT US 5317196 A US 1992-936445 19920828; JP 06177279 A JP 1993-216857 19930810
PRAI US 1992-936445 19920828
AB US 5317196 A UPAB: 19961211
An article comprises an electronic device enclosed in a contained fluid encapsulant comprising a silicone resin from polydimethylsiloxane

polymethylphenylsiloxane and/or polydimethyldiphenylsiloxane, terminated with vinyl and hydride components in a ratio of 5-20:1, and a catalyst from Pt and Sn.

USE/ADVANTAGE - Esp. in the prodn. of flip-**chip** surface mounted **integrated circuit** subjected to relatively high voltages and wide temp. changes. The ratio of hydride and vinyl termination ensures that the encapsulant remains **liq**. even after **cure**, providing dependable **insulation** under high voltages and avoiding differential expansion effects on the solder bonds.

L12 ANSWER 26 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1995-055171 [08] WPIX
DNN N1995-043361 DNC C1995-025037
TI Wiring harness for cars - unified with grommet.
DC A32 A85 X12 X22
PA (FURU) FURUKAWA ELECTRIC CO LTD
CYC 1
PI JP 06333433 A 19941202 (199508)* 11p
ADT JP 06333433 A JP 1993-139979 19930519
PRAI JP 1993-139979 19930519
AB JP 06333433 A UPAB: 19950301
The wiring harness unified with a grommet comprises the harness (12) composed of a wire bundle, and a grommet (14) for holding the wire bundle passed through the hole of partition wall. The grommet (14) comprises the head part (18) and the fitting part (22) to fit with the partition wall. The head part (18) of the grommet (14) comprises the periphery part (18A) surrounded the wiring harness (12) and the central part (18B) filling the gaps between wires (16) of the bundle. The periphery part (18A) and central part (18B) are formed with the same material.

(1) The material comprises **cured liquid** resin. (2), esp. polyurethane resin. (3) The moulding **die** comprises an upper mould (30) and a lower mould (40) forming **cavity** (50) to mould the grommet with the wiring harness. The **cavity** (50) comprises the grommet part (32) having the same outline as the grommet (14), and the upper through-hole (33) extending upward and the lower through-hole (46) extending downward to pass through the wiring harness.

L12 ANSWER 32 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1993-160725 [20] WPIX
DNN N1993-123361 DNC C1993-070929
TI Conformal coating compsns. - prepd. from liq. hydrocarbon diol(s) and/or their derivs. and cycloaliphatic epoxide(s).
DC A21 A28 A82 A85 G02 L03 V04
IN ARGYROPOULOS, J N; BASSETT, D R; KOLESKE, J V; SMITH, O W
PA (UNIC) UNION CARBIDE CHEM & PLASTICS
CYC 13
PI EP 542218 A1 19930519 (199320)* EN
R: AT BE DE DK ES FR GB IT NL SE
BR 9204385 A 19930601 (199326)
CA 2082563 A 19930513 (199330)
JP 05239402 A 19930917 (199342) 20p
AB EP 542218 A UPAB: 19931116
A curable conformal coating compsn. comprises (A) a liq. hydrocarbon diol and/or its deriv. and (B) a cycloaliphatic epoxide. (A) comprises prim. OH gps. and 8 or more C in which the OH gps. are sepd. by 4 or more C arranged linearly. At least one C is a disubstd. C, or, at least 2C are monosubstd. (A) exists as a liq. at 35 deg.C or less. The compsn. pref. further contains an epoxide (different from (B)), a polyol (different from (A)), a vinyl ester, a surfactant, a flow and levelling agent, an onium salt photoinitiator, a triflic acid salt or block Bronsted acid, and a fluorescent dye.

Also claimed are: (1) a cured film prepd. from the described compsn. (2) a printed circuit board coated with the cured compsn.

USE/ADVANTAGE - The compsns. are used for coating various metal, ceramic, glass, plastic and composite substrates which may be in the form of printed wired circuit boards, printed circuit assembly, of electrical components, semiconductor **chips** and other parts used in the electronics industry. Coating is such that an **encapsulated** system is provided. A stable compsn. is provided. The compsns. are curable by UV radiation and/or thermal energy, have improved moisture resistance and odour properties. Electrical resistance is good as are **dielectric** properties, including **dielectric** breakdown voltage. The compsns. are not partic. irritating or sensitising. Properties are developed rapidly, and the **liq**. coatings are **cured** to a tack-free state after a few secs. or less. On curing to provide an **encapsulated** system, the coatings give **protection** against high humidity conditions, standing water or snow, high temp., dust ionic contaminants, fungi and mildew. The coatings burn cleanly without charring during repair or arcing on the board.
Dwg.0/0

L12 ANSWER 33 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1993-060218 [08] WPIX
DNN N1993-045987 DNC C1993-026860
TI Formation of electrical via through circuit **package** - by coating substrate opening with **dielectric** then reopening and applying conductive coating.
DC A85 L03 U11 U12 X15
IN CAVICCHI, B T; MASON, A V
PA (SPEC-N) SPECTROLAB INC
CYC 8
PI EP 528311 A2 19930224 (199308)* EN 13p <--
AU 9220907 A 19930225 (199315) <--
EP 528311 A3 19930303 (199349) <--
JP 05326991 A 19931210 (199403) 8p <--

AU 648921 B 19940505 (199423) <--
US 5425816 A 19950620 (199530) 12p <--
EP 528311 B1 19970108 (199707) EN 15p <--

AB EP 528311 A UPAB: 19940126
The via is formed by making an opening (48) through the **package** substrate, coating and closing the opening with **dielectric** material (52), making a second opening through the **dielectric**, and coating the **dielectric** with conductive material (54) which extends between the opposite sides of the substrate and is **insulated** from it by the **dielectric**.

The **dielectric** is pref. applied as a **liq**. and then **cured** to solid state, and is, e.g., polyimide. In partic., the **package** is a solar cell with electrical contact layers on the front and back faces, and the conductive coating is formed simultaneously with the front contact layer as a unitary layer.

L12 ANSWER 34 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1992-208424 [25] WPIX
CR 1991-339231 [46]
DNN N1992-157933 DNC C1992-094681
TI Appts. for forming interconnections between and **IC** and **package** - comprises packaging means for support, non-conductive organic polymer covering **package** and connector providing electrical coupling between **IC** and **package**.
DC A85 L03 U11
IN KELLEY, E P; QUEEN, W D
PA (USNA) US SEC OF NAVY
CYC 1
PI US 5119173 A 19920602 (199225)* 5p <--
ADT US 5119173 A Div ex US 1990-557449 19900718, US 1991-714813 19910613
FDT US 5119173 A Div ex US 5061657
PRAI US 1990-557449 19900718; US 1991-714813 19910613
AB US 5119173 A UPAB: 19931006
Integrated circuit (10) is placed in a **cavity** (12) of a support **package** (14), a non conductive organic polymer is provided to cover the **package** and contact areas (16,18) on both the **integrated circuit** and the **package**, and conductive connections are formed in the organic polymer between the contact areas (16,18) on the circuit and **package**.

The conductive paths between the **IC** contacts (16) and the **package** contacts (18) are pref. formed by chemical doping, focussed ion beam doping, or direct ion beam doping of the non-conductive organic polymer. The organic polymer can be **cured liq**. organic polymer or an electrochemically deposited or low pressure chemical vapour deposited layer of polyacetylene, poly (p-phenylene sulphide) or (2,6-dimethylphenylene-**oxide**). An additional layer of non conductive polymer can be formed over the first layer with a cover over the additional layer.

L12 ANSWER 35 OF 44 JAPIO COPYRIGHT 2002 JPO
AN 1990-233383 JAPIO
TI HEAT **INSULATING** CONTAINER AND ITS MANUFACTURE
IN TERANISHI KOICHIRO; YAMAZAKI TAKASHI; MINAKI AKITO
PA MEISEI KOGYO KK, JP (CO 414929)
PI JP 02233383 A 19900914 Heisei
AI JP1989-52636 (JP01052636 Heisei) 19890304
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 1055, Vol. 14, No. 549, P. 112 (19901206)
AB PURPOSE: To prevent the lowering of heat **insulating** performance

due to the intrusion of water, etc., in order to obtain an excellent water resisting and heat **insulating** ability by embedding a vacuum **insulating** panel in a container with the simultaneous molding thereof and sealing said vacuum **insulating** panel in a synthetic resin wall enclosure for the **protective** purpose and in a highly air tight condition.
CONSTITUTION: A heat **insulating** container consists of a vacuum **insulating** panel 1 having a thickness of 15 mm enclosed in a polyurethane resin wall enclosure 2 forming RIM and having a thickness of 3mm. A method of forming the vacuum **insulating** panel 1 excellent in **insulative** ability comprises the steps of filling superfine substances excellent in heat **insulating** performance in an airtight container composed of a high gas-barrier laminate film, evacuating said container, anchoring the heat **insulating** panel 1 securely in a position spaced from the inner walls of a metal **die** 3, introducing a mixture of **liquid** resins A and **curing** material B into said metal **die** 3, causing the curing reaction to take place therein, removing the molded vacuum **insulating** panel 1 therefrom and embedding said **insulating** panel 1 in the wall enclosure.

L12 ANSWER 36 OF 44 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1990-277079 [37] WPIX
CR 1990-180640 [24]
DNN N1990-214119 DNC C1990-119700
TI Connecting semiconductor **chip** to PCB - using **insulating** , heat and pressure **curable** adhesive film contg. **liq.** epoxy resin, solid resin and microcapsule type curing agent.
DC A21 A85 G03 L03 U11 U14
IN GOTO, Y; NAKAJIMA, A; TSUKAGOSHI, I; YAMAGUCHI, Y
PA (HITB) HITACHI CHEM CO LTD
CYC 7
PI EP 387066 A 19900912 (199037)*
R: DE FR GB NL
JP 03016147 A 19910124 (199110)
EP 387066 B1 19940525 (199421) EN 21p <--
R: DE FR GB NL
DE 69009088 E 19940630 (199427) <--
KR 9310722 B1 19931108 (199439) <--
US 5843251 A 19981201 (199904)
US 6113728 A 20000905 (200044)

AB EP 387066 A UPAB: 20000913
Electrically connecting circuits in which at least one circuit is provided on an **insulating** layer and has projecting electrodes which are deformable under pressure in the circuit connecting operation involves the interposition between the circuits of an **insulating** heat and pressure curable adhesive film with less than 0.5 wt% volatile content, of less than 50 microns in thickness, and comprising (i) a liq. epoxy resin, (ii) a solid resin having at least one functional gp., and (iii) a microcapsule type curing agent.
ADVANTAGE - Application of heat and pressure to a sandwich consisting of a semiconductor **chip**, the adhesive film and a circuit on a substrate results in simultaneous electrical connection and bonding, with excess adhesive forming a **protective** bead round the **chip** . The characteristics of the adhesive permit live testing of the circuit while the adhesive is in a half-cured state (claimed). @(14pp Dwg.No.1a/8)@

L12 ANSWER 44 OF 44 JAPIO COPYRIGHT 2002 JPO
AN 2000-183279 JAPIO
TI **PACKAGE** FOR SEMICONDUCTOR ELEMENT AND MANUFACTURE THEREOF
IN NAGATOMO SUMI; YAMADA SHOJI; IKEDA YOSHINARI
PA FUJI ELECTRIC CO LTD
PI JP 2000183279 A 20000630 Heisei
AI JP1998-307608 (JP10307608 Heisei) 19981028
PRAI JP 1998-283076 19981005
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To reduce falling of bonding wires, generation of voids, warpage of a **package** due to a shrinkage in a molding resin and the like by a method, wherein a thermosetting resin layer is formed at normal temperature by a vacuum injection molding of a liquid thermosetting resin in such a way as to cover at least semiconductor **chips** and a lead frame.
SOLUTION: While a lead frame 4 mounted with semiconductor **chips** 3 is held by a hard plastic molded member, the lead frame 4 is combined with an Al plate 6 at 150°C in a vacuum of 0.3 Torrs, and the lead frame 4 is made to bond to the plate 6 without voids. At that time, a **liquid** heat-**cured** silicon bonding agent is coated in advance on the contact part of the molded member with the plate 6 and the molded member, and the plate 6 are made to bond together at the time of a vacuum bonding of the molded member to the plate 6. After an **insulating** layer 5 and the bonding part are **cured**, **liquid** vacuum injection molding is formed using a flexible resin at room temperatures to form a flexible resin layer 1, and the layer 1 is cured to manufacture a molded **package**. The **package** manufactured in this way satisfies the module characteristics, and a warpage of the **package** is reduced.
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